High-Efficiency Bridgeless Three-Level Power Factor Correction Rectifier

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***Abstract*—A high-efficiency bridgeless three-level power factor correction (PFC) rectifier is proposed. The circuit configuration of the proposed rectifier consists of four metal oxide semiconductor field-effect transistor (MOSFET) switches, and the reverse recovery problems of the switches are eliminated. Also, the proposed rectifier with three voltage levels reduces the power losses, harmonic components, voltage ratings, and electromagnetic interference. To control the grid current and the output voltage effectively, a feed-forward nominal voltage compensator with the mode selector is developed; by presetting the operating point of the grid voltage, this compensator improves the control environment. Thus, the proposed three-level PFC rectifier with developed control algorithm provides high power quality and high efficiency of 99.05%. Experimental results based on a 1-kW prototype are provided to evaluate its performance and verify the analysis.**

***Index Terms*—AC–DC power conversion, MOSFET-based rectifier, multilevel, single-phase.**

I. Introduction

TO INTERFACE with the grid, ac–dc rectifiers should consider compliance with international standards such as IEEE 519, IEC 1000-3-2, and EN 61000-3-2 [1]–[3]. In these compliance, the rectifiers are required to achieve both high-power factor (PF) and low total harmonic distortion (THD) for enhancing the power quality of the grid [4]. The simplest way for satisfying the requirements is to use the passive PFC rectifiers which consist of only the passive filters. However, the passive PFC rectifiers cannot provide the sufficient high-power quality, and they are too large and heavy [5], [6]. Two-stage PFC rectifiers have been developed in [7] and [8] to overcome the drawbacks of passive PFC rectifiers. Two-stage PFC rectifiers consist of a front-end ac–dc PFC rectifier and a dc–dc converter. The front-end ac–dc PFC rectifier controls the grid current to be in phase with the grid voltage, and the other stage performs the output control and gives galvanic isolation. This structure has the advantages of providing high PF and wide input range operating performance. However, because of two respective power-processing stages, these rectifiers have a high system complexity and low efficiency [9], [10]. In single-stage PFC rectifiers, the front-end ac–dc PFC rectifier and the dc–dc converter are integrated into one power-processing stage; by sharing the switches, they decrease the system complexity [11]–[13]. They also have a smaller volume compared to the two-stage PFC rectifiers [14]. However, the semiconductor devices of the single-stage PFC rectifiers suffer from the excessive voltage and current stresses, and these rectifiers have the burden of the high conduction losses [15]. For the improvement of the efficiency and the power quality, the multilevel PFC rectifiers have been considered as a solution in many literatures [16]–[20]. Their main advantages are characterized by the lower switching losses and lower harmonic components compared to two-level rectifiers. However, many of the multilevel PFC rectifiers have a full-bridge diode rectifier and the reverse recovery problem of the MOSFET body diodes. The full-bridge diode rectifier significantly increases the conduction losses, and the reverse recovery problems also decrease the efficiency.

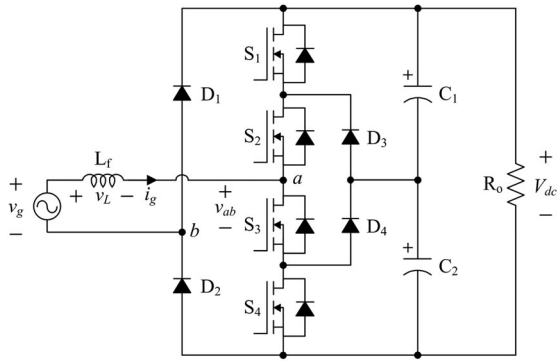

Fig. 1. Circuit diagram of the proposed rectifier.

This paper proposes a high-efficiency bridgeless three-level PFC rectifier. The proposed rectifier minimizes the overall power losses by eliminating the full-bridge diode rectifier and the reverse recovery problems of the MOSFET body diodes. Also, the proposed rectifier with three voltage levels reduces the power losses, harmonic components, voltage ratings, and electromagnetic interference; it allows the use of the small and cheap filters. To control the grid current and the output voltage effectively, the feed-forward nominal voltage compensator with the mode selector is developed. The feed-forward nominal voltage compensator improves the control environment by presetting the operating point of the grid voltage. Thus, the

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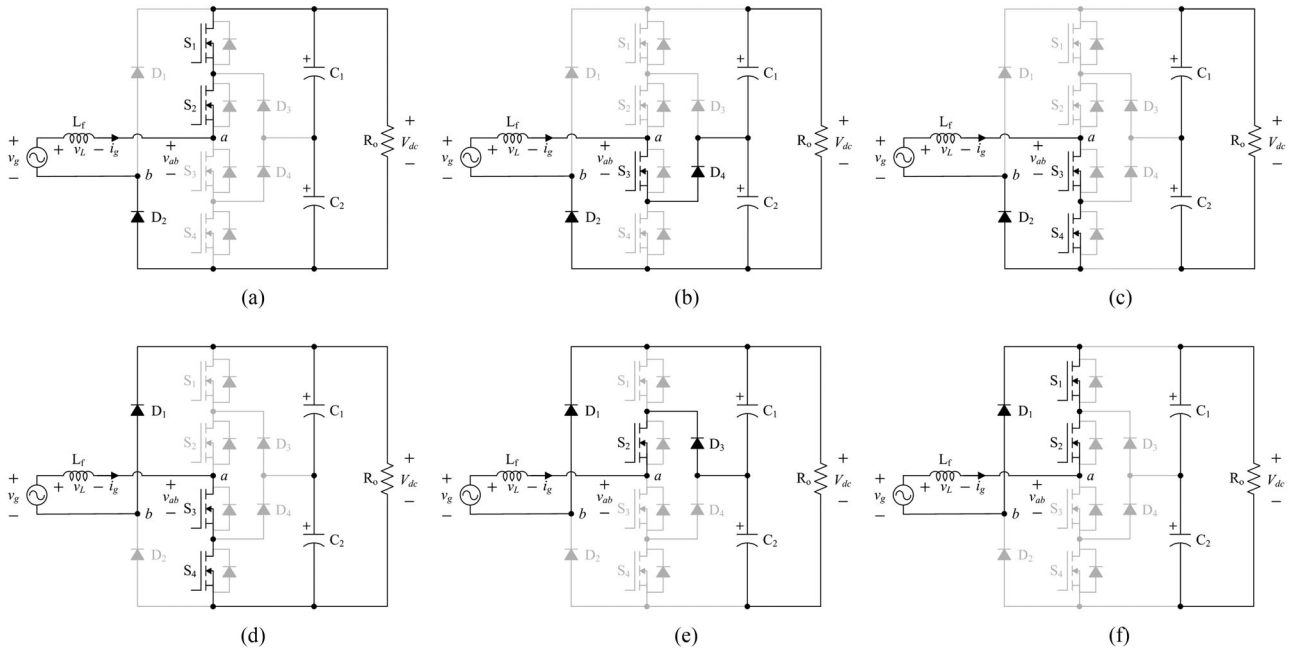

Fig. 2. Operation circuit diagrams of the proposed rectifier under the following conditions: (a) $v_{ab} = V_{dc}, v_g > 0, i_g > 0$. (b) $v_{ab} = V_{dc}/2, v_g > 0, i_g > 0$. (c) $v_{ab} = 0, v_g > 0, i_g > 0$. (d) $v_{ab} = -V_{dc}, v_g < 0, i_g < 0$. (e) $v_{ab} = -V_{dc}/2, v_g < 0, i_g < 0$. (f) $v_{ab} = 0, v_g < 0, i_g < 0$. Current flows only along lines drawn in black.

proposed three-level PFC rectifier provides high efficiency and high power quality. The experimental results show the validity of the proposed rectifier.

II. Operation Principles and Control Algorithm of Proposed Rectifier

The proposed rectifier shown in Fig. 1 consists of two dc-link capacitors C_1 and C_2, two high-voltage rating diodes D_1 and D_2, two low-voltage rating diodes D_3 and D_4, four switches S_1–S_4, and one filter inductor L_f. The circuit configuration of this rectifier is composed of two legs: one leg that has two high-voltage rating diodes; the other leg that has a three-level voltage cell. Two high-voltage rating diodes D_1 and D_2 conduct alternately during one grid period; the bottom diode D_2 conducts during the positive half-cycle of the grid voltage, and the top diode D_1 conducts during the negative half-cycle. Three-level voltage cell operates at high frequency and provides three voltage levels.

S_1 and S_3 operate complementarily to each other, and S_2 and S_4 also operate complementarily to each other. Therefore, just two duty ratios are required to control the proposed rectifier; the steady-state duty D_{n1} is the duty ratio of S_1, and the steady-state duty D_{n2} is the duty ratio of S_2. As shown in Fig. 2, the possible number of switching states is six; because the repeated zero-voltage level is counted as just one level, a total of five voltage levels are provided at five-level voltage v_{ab} ($V_{dc}, V_{dc}/2, 0, -V_{dc}/2, -V_{dc}$, where V_{dc} is the output voltage). The grid voltage v_g can be divided into four sections according to the five voltage levels, and these sections decide the switching modes: mode 1 ($V_{dc}/2 < v_g < V_{dc}$), mode 2 ($0 < v_g < V_{dc}/2$), mode 3 ($-V_{dc}/2 < v_g < 0$), and mode 4 ($-V_{dc} < v_g < -V_{dc}/2$). The voltage comparison should be proceeded to select the mode, and this selecting process is performed by the mode selector shown in Fig. 3.

In mode 1, S_1 and S_3 operate at high frequency; Fig. 2(a) and (b) shows the operation circuit diagram in mode 1. During the on-state and off-state of S_1, the inductor voltage v_L is obtained as

$$v_L = v_g - V_{dc}, \qquad \text{on-state of } S_1 \tag{1}$$

$$v_L = v_g - \frac{V_{dc}}{2}, \qquad \text{off-state of } S_1 \tag{2}$$

where $v_L < 0$ at on-state, and $v_L > 0$ at off-state; mode 1 has the operation voltage range ($V_{dc}/2 < v_g < V_{dc}$) as shown in Fig. 4. Because of the principle of the inductor volt-second balance, the steady-state duty D_{n1} of S_1 can be obtained as

$$D_{n1}(v_g - V_{dc}) + (1 - D_{n1})\left(v_g - \frac{V_{dc}}{2}\right) = 0 \tag{3}$$

$$D_{n1} = \frac{2v_g}{V_{dc}} - 1. \tag{4}$$

In contrast, S_2 has a fixed duty ratio D_{n2} given as follows:

$$D_{n2} = \frac{t_{swon}}{T_s} = \frac{T_s}{T_s} = 1 \tag{5}$$

where t_{swon} is on-time during the switching period, and T_s is the switching period. Thus, by the above processes, two duty ratios in all modes can be obtained as

$$D_{n1} = \frac{2v_g}{V_{dc}} - 1, \quad D_{n2} = 1, \qquad \text{for mode 1} \tag{6}$$

$$D_{n1} = 0, \qquad D_{n2} = \frac{2v_g}{V_{dc}}, \qquad \text{for mode 2} \tag{7}$$

$$D_{n1} = \frac{2v_g}{V_{dc}} + 1, \quad D_{n2} = 1, \qquad \text{for mode 3} \tag{8}$$

$$D_{n1} = 0, \qquad D_{n2} = \frac{2v_g}{V_{dc}} + 2, \qquad \text{for mode 4.} \tag{9}$$

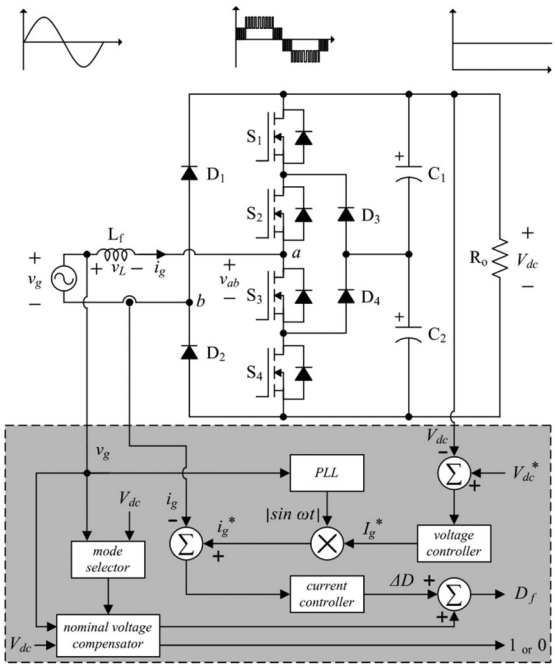

Fig. 3. Overall control system block diagram of the proposed rectifier.

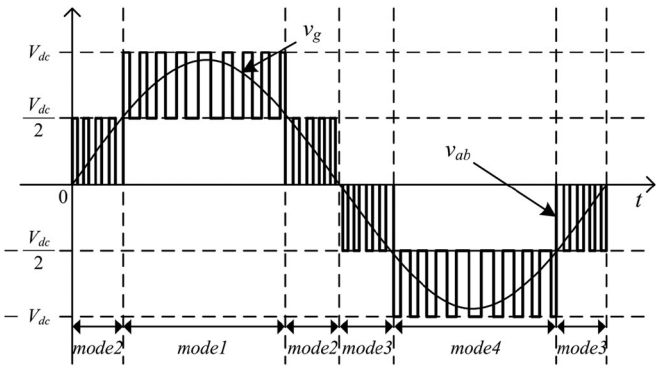

Fig. 4. Five-level voltage v_{ab} and grid voltage v_g waveform.

Unlike the above steady-state condition, to control the grid current i_g, the control duty ΔD must be added at the steady-state duty. However, it will be discussed in detail only for mode 1 because ΔD is computed in exactly the same way for all four modes. As shown inFig. 4, switching frequency f_s is much higher than grid frequency f_g. Therefore, the grid voltage v_g can be considered constant voltage during the switching period T_s, as shown in Fig. 5. In mode 1, as shown in Fig. 5, the averaged equation for the filter inductance L_f over one switching period can be derived as

$$D_f(v_g - V_{\rm dc}) + (1 - D_f)\left(v_g - \frac{V_{\rm dc}}{2}\right) = L_f \frac{\Delta i_g}{T_s} \tag{10}$$

where D_f is the final control duty and Δi_g is the variation of the grid current. The averaged equation in (10) can be rearranged to

$$D_f = \left(\frac{2v_g}{V_{\rm dc}} - 1\right) - \frac{2L_f \Delta i_g}{V_{\rm dc} T_s}. \tag{11}$$

The first term in (11) is the same as the steady-state duty D_{n1} at mode 1 switching operation. Thus, the second term in (11) can

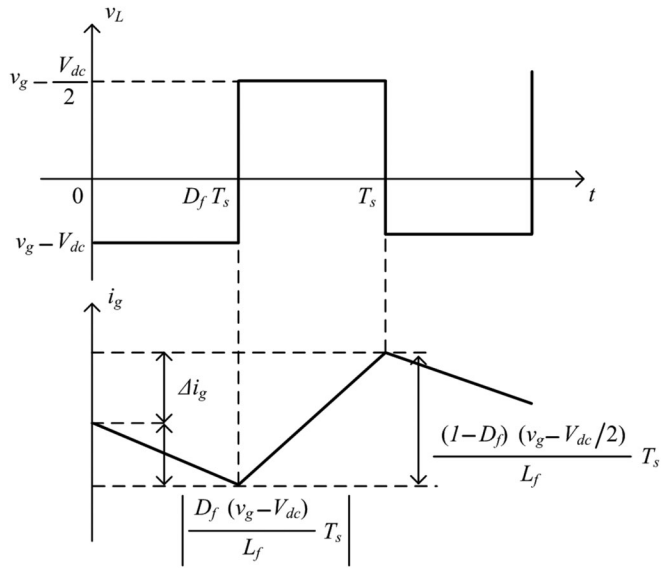

Fig. 5. Inductor current and voltage waveforms of the proposed rectifier in mode 1.

be defined as

$$\Delta D = -\frac{2L_f \Delta i_g}{V_{\rm dc} T_s}. \tag{12}$$

As a result of two re-expressed terms, (11) is represented in sum of two duty terms

$$D_f = D_{n1} + \Delta D. \tag{13}$$

The second term ΔD directly contributes to the grid current control; this term is used to track the grid current reference i_g^* and is obtained from a current controller.

In view of the overall system, the control block diagram of the proposed rectifier is shown in Fig. 3. The output voltage controller is involved in controlling the grid current reference amplitude I_g^*, and the proportion of the controlling is decided by the difference of the output voltage reference $V_{\rm dc}^*$ and the output voltage $V_{\rm dc}$. It consequently affects the output voltage regulation. The developed final control duty D_f consists of the steady-state duty D_{n1} and the control duty ΔD. D_{n1} is used as the feed-forward nominal voltage compensator, and it improves the control environment by presetting the operating point. ΔD directly contributes to the grid current control and is used to track the grid current reference i_g^*. As a result of those developed controllers, the proposed rectifier performs precise reference current tracking, and the output voltage maintains constant.

III. Semiconductor Device Power Loss Analysis

The semiconductor devices of the proposed rectifier consist of S_1–S_4 that operate at switching frequency f_s, D_1 and D_2 that conduct during the half-cycle of the grid period, and D_3 and D_4 that conduct according to the on-time or off-time of the switching period. The power loss analysis is provided, in which the grid voltage v_g, grid frequency f_g, switching frequency f_s, and rated power P_o are 220 $V_{\rm rms}$, 60 Hz, 20 kHz, and 1 kW,

TABLE I
PARAMETERS AND COMPONENTS OF PROTOTYPE

Parameters	Symbols	Value
Rated power	P_o	1 kW
Output voltage	$V_{\rm dc}$	380 V
Grid voltage	v_g	176–264 $V_{\rm rms}$
Grid frequency	f_g	60 Hz
Switching frequency	f_s	20 kHz
DC-link capacitance	C_1, C_2	940 μF
Filter inductance	L_f	1 mH
Components	Symbols	Part number
Main switches	S_1-S_4	IRFP4668PbF
High-voltage rating diodes	D_1, D_2	VS-30CPU04P
Low-voltage rating diodes	D_3, D_4	DSSK60-02A

respectively. The detailed system parameters and components are listed in Table I.

S_1-S_4 have no reverse recovery losses because they do not use the body diodes in any operations as shown in Fig. 2. Also, D_1 and D_2 have very minor reverse recovery losses because they conduct at grid frequency f_g. Furthermore, D_3 and D_4 have almost zero reverse recovery loss because of the characteristics of Schottky diodes; they do not have a recovery time. Therefore, the proposed rectifier has to consider only the conduction losses of all the diodes without the consideration of reverse recovery losses. The operation principles of the proposed rectifier are based on the assumptions that the rectifier has the unity PF. Thus, the grid voltage v_g and the grid current i_g can be obtained as

$$v_g = V_g \sin(2\pi f_g t) \tag{14}$$

$$i_g = I_g \sin(2\pi f_g t) \tag{15}$$

where V_g is the peak value of the grid voltage, and I_g is the peak value of the grid current. For the precise loss analysis, time t can be sampled by the switching period T_s; $t = kT_s$, where k is the switching period sampling number in the grid period. Five-level voltage $v_{\rm ab}$ and the grid voltage v_g waveform with four-mode switching operation are shown in Fig. 4. Diode conduction losses at k-th switching period are the average dissipated power during the forward conduction phase given in

$$W_{d,\rm con}[k] = V_F i_{d,\rm avg}[k] D_f[k] T_s \tag{16}$$

where V_F is forward voltage of a diode, and $i_{d,\rm avg}[k]$ is the k-th average diode current. For (16), diode current waveform should be approximated as a square waveform.

S_1-S_4 should consider both switching losses and conduction losses. At the k-th switching moment, the switching losses of S_1-S_4 are computed from the cross region; the drain-to-source voltage $V_{\rm ds}$ and the switch current i_s intersect at the switch turns ON and OFF moment. This cross region can be approximated as a triangular shape. Therefore, the k-th on-time or off-time switching losses are derived as

$$W_{s,\rm swon}[k] = \frac{1}{2} V_{\rm ds} i_{\rm sw}[k] t_{\rm on} \tag{17}$$

$$W_{s,\rm swoff}[k] = \frac{1}{2} V_{\rm ds} i'_{\rm sw}[k] t_{\rm off} \tag{18}$$

TABLE II
POWER LOSSES OF SEMICONDUCTOR DEVICES

Major loss	Symbols	Value
Diodes conduction loss	D_1-D_4	4.75 W
Switches switching loss	S_1-S_4	1.47 W
Switches conduction loss	S_1-S_4	0.24 W

where $i_{\rm sw}[k]$ and $i'_{\rm sw}[k]$ are the switch currents at the switch turns ON and OFF moment, and $t_{\rm on}$ and $t_{\rm off}$ are the cross region times at the switch turns ON and OFF moment. The total of switching losses is the half of the conventional two-level rectifiers because $V_{\rm ds}$ in this proposed three-level rectifier is the half of two-level rectifier drain-to-source voltage. The k-th conduction losses of S_1-S_4 are computed as

$$W_{s,\rm con}[k] = (i_{s,\rm rms}[k])^2 R_{ds} T_s \tag{19}$$

where $R_{\rm ds}$ is static drain-to-source on-resistance, and $i_{s,\rm rms}[k]$ is the k-th rms value of switch current. The k-th switch current $i_s[k]$ is a trapezoidal waveform, so the rms value is obtained as

$$i_{s,\rm rms}[k] = \sqrt{\frac{\left(i_{\rm sw}[k]\right)^2 + \left(i'_{\rm sw}[k]\right)^2 + i_{\rm sw}[k] i'_{\rm sw}[k]}{3} D_f[k]}. \tag{20}$$

The result of power loss analysis of the semiconductor devices is shown in Table II . The sum of sampled equations is calculated using MATLAB. The proposed rectifier eliminates the reverse recovery problems of all the diodes, and S_2 and S_3 have no power losses during the switching operation in mode 2 and mode 3. Thus, this analysis verifies the validity of the high efficiency of the proposed rectifier.

IV. EXPERIMENTAL RESULT

The prototype for the proposed rectifier, shown in Fig. 1, is implemented to show the validity. The grid voltage v_g range, grid frequency f_g, and rated power P_o are 176–264 $V_{\rm rms}$, 60 Hz, and 1 kW, respectively. The detailed system parameters and components are listed in Table I.

Fig. 6 shows the experimental results for the five-level voltage $v_{\rm ab}$, the grid voltage v_g, the grid current i_g, and output voltage $V_{\rm dc}$ at full-load condition. Fig. 6(a) shows that the grid voltage v_g and the grid current i_g are in phase, and the output voltage $V_{\rm dc}$ remains constant at the grid voltage 264 $V_{\rm rms}$. Also, at the grid voltage 220 and 176 $V_{\rm rms}$, Fig. 6(b) and (c) shows that the grid voltage v_g and the grid current i_g are in phase, and the output voltage $V_{\rm dc}$ remains constant. The grid current has a sinusoidal form and desired rated power level P_o in each grid voltage condition.

Fig. 7 shows the measured efficiency under entire load conditions at each grid voltage v_g condition. It verifies that the proposed rectifier provides high efficiency, and measured maximum efficiency is 99.05% at the full-load condition with the rated grid voltage. To understand the merits of the proposed rectifier, the measured efficiency can be compared with the measured efficiencies of conventional rectifiers in [21]–[24]. In Fig. 8, total five efficiencies are compared at each load condition to show the result explicitly. As a result of the comparison, it is clear

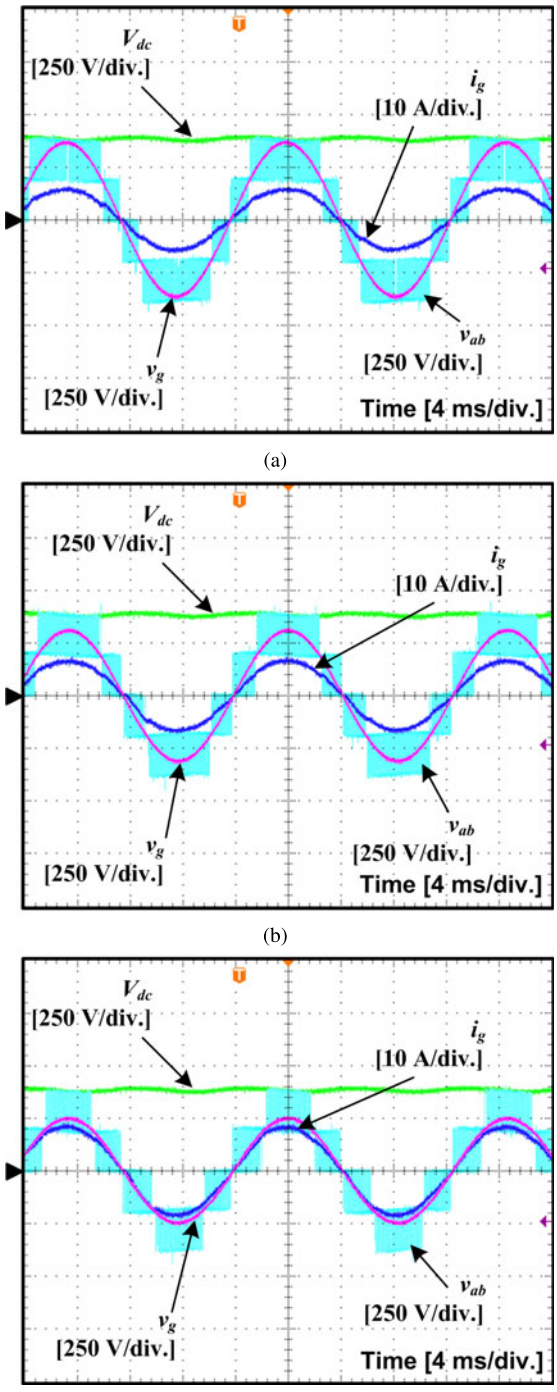

Fig. 6. Experimental result of the five-level voltage v_{ab}, the grid voltage v_g, the grid current i_g, and output voltage V_{dc} at the full-load condition. (a) v_g = 264 V_{rms}. (b) v_g = 220 V_{rms}. (c) v_g = 176 V_{rms}.

that the proposed rectifier has higher efficiency than those of the conventional rectifiers under 1 kW load conditions. This result shows that the proposed rectifier significantly reduces power losses.

Figs. 9 and 10 verify that the proposed rectifier provides high power quality. As shown in Fig. 9, the proposed rectifier satisfies the international standards EN 61000-3-2 Class A standard, and the THD is measured less than 4% under full-load condition.

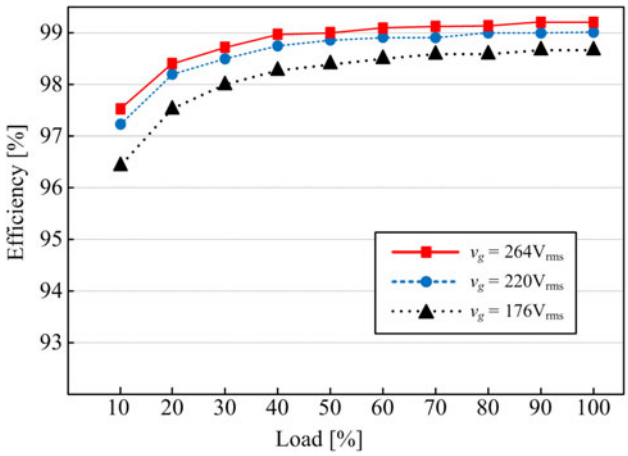

Fig. 7. Measured efficiency under entire load conditions at each grid voltage v_g condition.

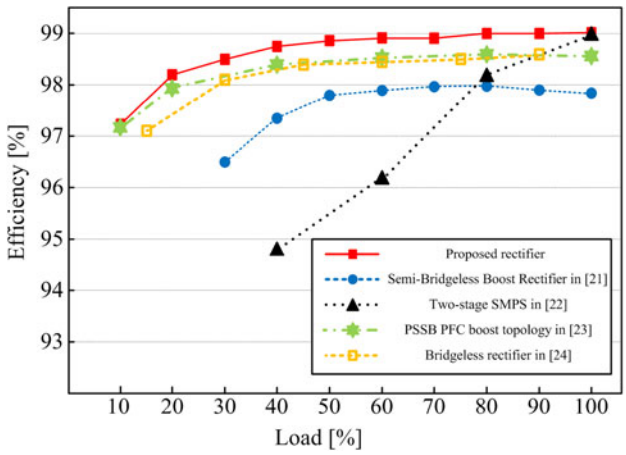

Fig. 8. Measured rectifier efficiencies at each load condition for power efficiency comparison with conventional rectifiers at the rated grid voltage.

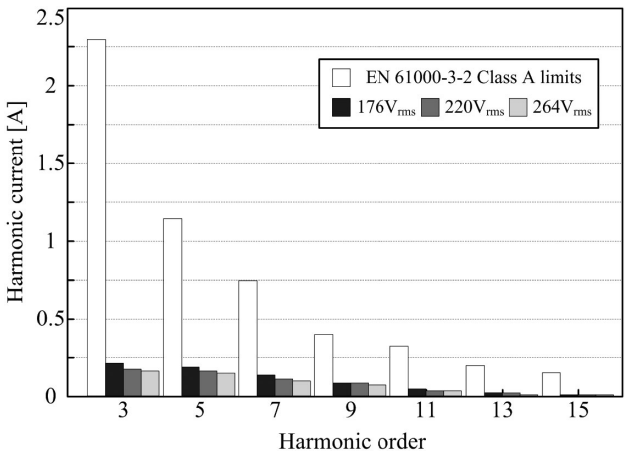

Fig. 9. Amplitude of harmonic current.

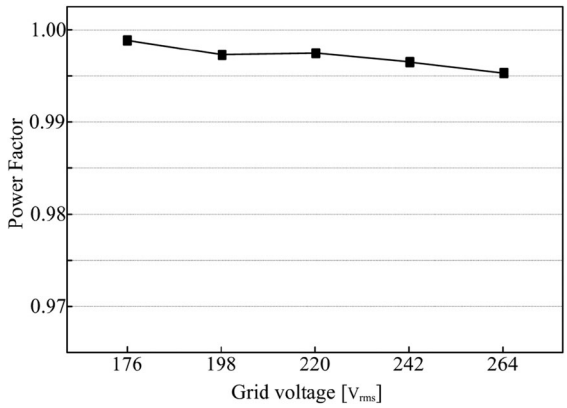

Fig. 10. Measured PF at each grid voltage v_g condition with the full-load condition.

At each grid voltage condition, the measured PF is above 0.99 as shown in Fig. 10. Measured maximum efficiency is 99.05%, measured maximum PF is 0.997, and measured minimum THD is 3.5% at the rated grid voltage and 1 kW rated power condition.

V. Conclusion

A high-efficiency bridgeless three-level PFC rectifier and a control system were introduced, and theoretical analysis and experimental results were also represented. By using the novel configuration, the proposed rectifier performs the power conversion through one power-processing stage with high efficiency and low harmonic components. Also, the proposed rectifier minimizes the overall power losses by eliminating the full-bridge diode rectifier and the reverse recovery problems of the MOSFET body diodes. Furthermore, the proposed rectifier with three voltage levels reduces the power losses, harmonic components, voltage ratings, and electromagnetic interference; it also allows the use of the small and cheap filters. The control algorithm with the feed-forward nominal voltage compensator improves the control environment by presetting the operating point of the grid voltage. Thus, the proposed high-efficiency three-level PFC rectifier provides high efficiency and high power quality, and its developed control algorithm gives the feasibility to the proposed rectifier. From the experimental results, using 1 kW prototype, it is verified that the proposed rectifier has high power quality with higher efficiency than the conventional PFC rectifiers, and the developed control system is suitable for the proposed rectifier.

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